CLAIMS

We claim:

1. A method of forming a double-gated transistor, comprising the sequential steps of:

providing a substrate having an SOI structure formed thereover; the SOI structure including a lower SOI oxide layer and an upper SOI silicon layer;

patterning the SOI silicon layer to form a patterned SOI silicon layer; the patterned SOI silicon layer including a source region and a drain region connected by a channel portion;

forming an encasing oxide layer over the patterned SOI silicon layer to form an encased patterned SOI silicon layer;

forming a patterned dummy layer over the encased patterned SOI silicon layer; the patterned dummy layer having an opening, with exposed side walls, exposing:

the channel portion of the encased patterned SOI silicon layer;

and

portions of the upper surface of the SOI oxide layer;

forming offset spacers over the exposed side walls of the patterned dummy layer opening;

etching the SOI oxide layer while minimizing the undercut portions of the upper surface of the SOI oxide layer into the SOI oxide layer to form a minimal undercut portions; the minimizing undercutting process also removing the offset spacers and the encasing oxide layer over the channel portion of the patterned SOI silicon layer;

forming a conformal oxide layer around the channel portion of the patterned SOI silicon layer;

forming a gate within the patterned dummy layer opening; the gate including an upper gate above the patterned SOI silicon layer and a lower gate under the patterned SOI silicon layer; and

removing the patterned dummy layer to form the double-gated transistor.

2. The method of claim 1, wherein the structure is a semiconductor substrate.

3. The method of claim 1, wherein the structure is comprised of silicon or germanium.

4. The method of claim 1, wherein the lower SOI oxide layer has a thickness of from about 1000 to 5000Å; the upper SOI silicon layer has a thickness of from about 300 to 2000Å; the encasing oxide layer has a thickness of from about 5 to 200Å; the patterned dummy layer has a thickness of from about 1000 to 3000Å; and the conformal oxide layer has a thickness of from about 5 to 200Å.

5. The method of claim 1, wherein the lower SOI oxide layer has a thickness of from about 2000 to 4000Å; the upper SOI silicon layer has a thickness of from about 500 to 1500Å; the encasing oxide layer has a thickness of from about 10 to 50Å; the patterned dummy layer has a thickness of from about 1500 to 2500Å; and the conformal oxide layer has a thickness of from about 10 to 50Å.

6. The method of claim 1, wherein the undercut portions are each from about 500 to 3000Å deep.

7. The method of claim 1, wherein the undercut portions are each from about 1000 to 2000Å deep.

8. The method of claim 1, wherein the undercut portions each protrude from about 0 to 2000Å under the patterned dummy layer opening.

9. The method of claim 1, wherein the undercut portions each protrude from about 0 to 500Å under the patterned dummy layer opening.

10. The method of claim 1, wherein the patterned dummy layer is comprised of nitride, silicon nitride or silicon oxynitride; and the gate is comprised of polysilicon, tungsten, W-Si_x or aluminum.

11. The method of claim 1, wherein the patterned dummy layer is comprised of nitride; and the gate is comprised of polysilicon.

12. The method of claim 1, wherein the undercut portions are formed using a dilute HF etch and the patterned dummy layer is removed using hot phosphoric acid.

13. The method of claim 1, wherein the encasing oxide layer and the conformal oxide layer are each formed by a growth process.

14. The method of claim 1, including the step of forming source/drain implants into the respective source region and the drain region to form a source and a drain after removal of the patterned dummy layer.

15. The method of claim 1, including the step of performing:

LDD implants; and

source/drain implants

after removal of the patterned dummy layer.

16. The method of claim 1, wherein the upper gate has exposed side walls and including the step of forming spacers over the upper gate exposed side walls after removal of the patterned dummy layer.

17. The method of claim 1, including the further step of then performing a salicidation process.

18. A method of forming a double-gated transistor, comprising the sequential steps of:

providing a substrate having an SOI structure formed thereover; the SOI structure including a lower SOI oxide layer and an upper SOI silicon layer;

patterning the SOI silicon layer to form a patterned SOI silicon layer; the patterned SOI silicon layer including a source region and a drain region connected by a channel portion;

forming an encasing oxide layer over the patterned SOI silicon layer to form an encased patterned SOI silicon layer;

forming a patterned dummy layer over the encased patterned SOI silicon layer; the patterned dummy layer having an opening, with exposed side walls, exposing:

the channel portion of the encased patterned SOI silicon layer; and

portions of the upper surface of the SOI oxide layer;

forming offset spacers over the exposed side walls of the patterned dummy layer opening;

etching the SOI oxide layer while minimizing the undercut portions of the upper surface of the SOI oxide layer into the SOI oxide layer to form a minimal undercut portions; the minimizing undercutting process also removing the offset spacers and the encasing oxide layer over the channel portion of the patterned SOI silicon layer; wherein the undercut portions each protrude from about 0 to 2000Å under the patterned dummy layer opening;

forming a conformal oxide layer around the channel portion of the patterned SOI silicon layer;

forming a gate within the patterned dummy layer opening; the gate including an upper gate above the patterned SOI silicon layer and a lower gate under the patterned SOI silicon layer; and

removing the patterned dummy layer to form the double-gated transistor.

19. The method of claim 18, wherein the structure is a semiconductor substrate.

20. The method of claim 18, wherein the structure is comprised of silicon or germanium.

21. The method of claim 18, wherein the lower SOI oxide layer has a thickness of from about 1000 to 5000Å; the upper SOI silicon layer has a thickness of from about 300 to 2000Å; the encasing oxide layer has a thickness of from about 5 to 200Å; the patterned dummy layer has a thickness of from about 1000 to 3000Å; and the conformal oxide layer has a thickness of from about 5 to 200Å.

22. The method of claim 18, wherein the lower SOI oxide layer has a thickness of from about 2000 to 4000Å; the upper SOI silicon layer has a thickness of from about 500 to 1500Å; the encasing oxide layer has a thickness of from about 10 to 50Å; the patterned dummy layer has a thickness of from about 1500 to 2500Å; and the conformal oxide layer has a thickness of from about 10 to 50Å.

23. The method of claim 18, wherein the undercut portions are each from about 500 to 3000Å deep.

24. The method of claim 18, wherein the undercut portions are each from about 1000 to 2000Å deep.

25. The method of claim 18, wherein the undercut portions each protrude from about 0 to 500Å under the patterned dummy layer opening.

26. The method of claim 18, wherein the patterned dummy layer is comprised of nitride, silicon nitride or silicon oxynitride; and the gate is comprised of polysilicon, tungsten, W-Si_x or aluminum.

27. The method of claim 18, wherein the patterned dummy layer is comprised of nitride; and the gate is comprised of polysilicon.

28. The method of claim 18, wherein the undercut portions are formed using a dilute HF etch and the patterned dummy layer is removed using hot phosphoric acid.

29. The method of claim 18, wherein the encasing oxide layer and the conformal oxide layer are each formed by a growth process.

30. The method of claim 18, including the step of forming source/drain implants into the respective source region and the drain region to form a source and a drain after removal of the patterned dummy layer.

31. The method of claim 18, including the step of performing:

LDD implants; and

source/drain implants

after removal of the patterned dummy layer.

32. The method of claim 18, wherein the upper gate has exposed side walls and including the step of forming spacers over the upper gate exposed side walls after removal of the patterned dummy layer.

33. The method of claim 18, including the further step of then performing a salicidation process.

34. A method of forming a double-gated transistor, comprising the sequential steps of:

providing a substrate having an SOI structure formed thereover; the SOI structure including a lower SOI oxide layer and an upper SOI silicon layer;

patterning the SOI silicon layer to form a patterned SOI silicon layer; the patterned SOI silicon layer including a source region and a drain region connected by a channel portion;

forming an encasing oxide layer over the patterned SOI silicon layer to form an encased patterned SOI silicon layer;

forming a patterned dummy layer over the encased patterned SOI silicon layer; the patterned dummy layer having an opening, with exposed side walls, exposing:

the channel portion of the encased patterned SOI silicon layer;

and

portions of the upper surface of the SOI oxide layer;

forming offset spacers over the exposed side walls of the patterned dummy layer opening;

etching the SOI oxide layer while minimizing the undercut portions of the upper surface of the SOI oxide layer into the SOI oxide layer to form a minimal undercut portions; the minimizing undercutting process also removing the offset spacers and the encasing oxide layer over the channel portion of the patterned SOI silicon layer; wherein the undercut portions are formed using a dilute HF etch;

forming a conformal oxide layer around the channel portion of the patterned SOI silicon layer;

forming a gate within the patterned dummy layer opening; the gate including an upper gate above the patterned SOI silicon layer and a lower gate under the patterned SOI silicon layer; and

removing the patterned dummy layer using hot phosphoric acid to form the double-gated transistor.

35. The method of claim 34, wherein the structure is a semiconductor substrate.

36. The method of claim 34, wherein the structure is comprised of silicon or germanium.

37. The method of claim 34, wherein the lower SOI oxide layer has a thickness of from about 1000 to 5000Å; the upper SOI silicon layer has a thickness of from about 300 to 2000Å; the encasing oxide layer has a thickness of from about 5 to 200Å; the patterned dummy layer has a thickness of from about 1000 to 3000Å; and the conformal oxide layer has a thickness of from about 5 to 200Å.

38. The method of claim 34, wherein the lower SOI oxide layer has a thickness of from about 2000 to 4000Å; the upper SOI silicon layer has a thickness of from about 500 to 1500Å; the encasing oxide layer has a thickness of from about 10 to 50Å; the patterned dummy layer has a thickness of from about 1500 to 2500Å; and the conformal oxide layer has a thickness of from about 10 to 50Å.

39. The method of claim 34, wherein the undercut portions are each from about 500 to 3000Å deep.

40. The method of claim 34, wherein the undercut portions are each from about 1000 to 2000Å deep.

41. The method of claim 34, wherein the undercut portions each protrude from about 0 to 2000Å under the patterned dummy layer opening.

42. The method of claim 34, wherein the undercut portions each protrude from about 0 to 500Å under the patterned dummy layer opening.

43. The method of claim 34, wherein the patterned dummy layer is comprised of nitride, silicon nitride or silicon oxynitride; and the gate is comprised of polysilicon, tungsten, W-Si_x or aluminum.

44. The method of claim 34, wherein the patterned dummy layer is comprised of nitride; and the gate is comprised of polysilicon.

45. The method of claim 34, wherein the encasing oxide layer and the conformal oxide layer are each formed by a growth process.

46. The method of claim 34, including the step of forming source/drain implants into the respective source region and the drain region to form a source and a drain after removal of the patterned dummy layer.

47. The method of claim 34, including the step of performing:

LDD implants; and

source/drain implants

after removal of the patterned dummy layer.

48. The method of claim 34, wherein the upper gate has exposed side walls and including the step of forming spacers over the upper gate exposed side walls after removal of the patterned dummy layer.

49. The method of claim 34, including the further step of then performing a salicidation process.